

V_{DRM}	= 5600	V	Phase Control Thyristor 5STP 03X6500
V_{DSM}	= 6500	V	
$I_{T(AV)M}$	= 350	A	
$I_{T(RMS)}$	= 550	A	
I_{TSM}	= 4.5×10^3	A	
$V_{(T0)}$	= 1.2	V	
r_T	= 2.3	mW	

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- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate

Blocking

Maximum rated values ¹⁾

Symbol	Conditions	5STP 03X6500	5STP 03X6200	5STP 03X5800
V_{DSM}, V_{RSM}	$f = 5 \text{ Hz}, t_p = 10 \text{ ms}$	6500 V	6200 V	5800 V
V_{DRM}, V_{RRM}	$f = 50 \text{ Hz}, t_p = 10 \text{ ms}$	5600 V	5300 V	4900 V
V_{RSM}	$t_p = 5 \text{ ms}, \text{ single pulse}$	7000 V	6700 V	6300 V
dV/dt_{crit}	Exp. to 3750 V, $T_{vj} = 125^\circ\text{C}$	1000 V/ μs		

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	I_{DSM}	$V_{DSM}, T_{vj} = 125^\circ\text{C}$			150	mA
Reverse leakage current	I_{RSM}	$V_{RSM}, T_{vj} = 125^\circ\text{C}$			150	mA

V_{DRM}/V_{RRM} are equal to V_{DSM}/V_{RSM} values up to $T_{vj} = 110^\circ\text{C}$

Mechanical data

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		8	10	12	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				0.4	kg
Housing thickness	H	$F_M = 10 \text{ kN}, T_a = 25^\circ\text{C}$	34.8		35.4	mm
Surface creepage distance	D_S		38			mm
Air strike distance	D_a		21			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

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On-state

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Average on-state current	$I_{T(AV)M}$	Half sine wave, $T_c = 70^\circ\text{C}$			350	A
RMS on-state current	$I_{T(RMS)}$				550	A
Peak non-repetitive surge current	I_{TSM}	$t_p = 10\text{ ms}$, $T_{vj} = 125^\circ\text{C}$, $V_D = V_R = 0\text{ V}$			4.5×10^3	A
Limiting load integral	$I^2 t$				101×10^3	A^2s
Peak non-repetitive surge current	I_{TSM}	$t_p = 8.3\text{ ms}$, $T_{vj} = 125^\circ\text{C}$, $V_D = V_R = 0\text{ V}$			4.85×10^3	A
Limiting load integral	$I^2 t$				98×10^3	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	$I_T = 1000\text{ A}$, $T_{vj} = 125^\circ\text{C}$			3.5	V
Threshold voltage	$V_{(TO)}$	$I_T = 300\text{ A} - 900\text{ A}$, $T_{vj} = 125^\circ\text{C}$			1.2	V
Slope resistance	r_T				2.3	$\text{m}\Omega$
Holding current	I_H	$T_{vj} = 25^\circ\text{C}$			80	mA
		$T_{vj} = 125^\circ\text{C}$			60	mA
Latching current	I_L	$T_{vj} = 25^\circ\text{C}$			500	mA
		$T_{vj} = 125^\circ\text{C}$			200	mA

Switching

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	$T_{vj} = 125^\circ\text{C}$, $I_{TRM} = 1000\text{ A}$, Cont. $f = 50\text{ Hz}$			100	$\text{A}/\mu\text{s}$
Critical rate of rise of on-state current	di/dt_{crit}	$V_D \leq 3750\text{ V}$, $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$ Cont. $f = 1\text{ Hz}$			1000	$\text{A}/\mu\text{s}$
Circuit-commutated turn-off time	t_q	$T_{vj} = 125^\circ\text{C}$, $I_{TRM} = 1000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -1\text{ A}/\mu\text{s}$, $V_D \leq 0.67 \cdot V_{DRM}$, $dv_D/dt = 20\text{ V}/\mu\text{s}$	700			μs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Recovery charge	Q_{rr}	$T_{vj} = 125^\circ\text{C}$, $I_{TRM} = 1000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -1\text{ A}/\mu\text{s}$	900		2000	μAs
Gate turn-on delay time	t_{gd}	$V_D = 0.4 \cdot V_{RM}$, $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$, $T_{vj} = 25^\circ\text{C}$			3	μs

Triggering

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Average gate power loss	$P_{G(AV)}$		see Fig. 9			

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate-trigger voltage	V_{GT}	$T_{vj} = 25\text{ °C}$			2.6	V
Gate-trigger current	I_{GT}	$T_{vj} = 25\text{ °C}$			400	mA
Gate non-trigger voltage	V_{GD}	$V_D = 0.4 \times V_{DRM}$, $T_{vj} = 125\text{ °C}$	0.3			V
Gate non-trigger current	I_{GD}	$V_D = 0.4 \times V_{DRM}$, $T_{vj} = 125\text{ °C}$	10			mA

Thermal

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}				125	°C
Storage temperature range	T_{stg}		-40		140	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double-side cooled $F_m = 8...12\text{ kN}$			45	K/kW
	$R_{th(j-c)A}$	Anode-side cooled $F_m = 8...12\text{ kN}$			85	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled $F_m = 8...12\text{ kN}$			95	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double-side cooled $F_m = 8...12\text{ kN}$			7.5	K/kW
	$R_{th(c-h)}$	Single-side cooled $F_m = 8...12\text{ kN}$			15	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^n R_{th i} (1 - e^{-t/t_i})$$

i	1	2	3	4
$R_{th i}(\text{K/kW})$	26.070	12.160	3.370	3.100
$\tau_i(\text{s})$	0.6439	0.0812	0.0161	0.0075

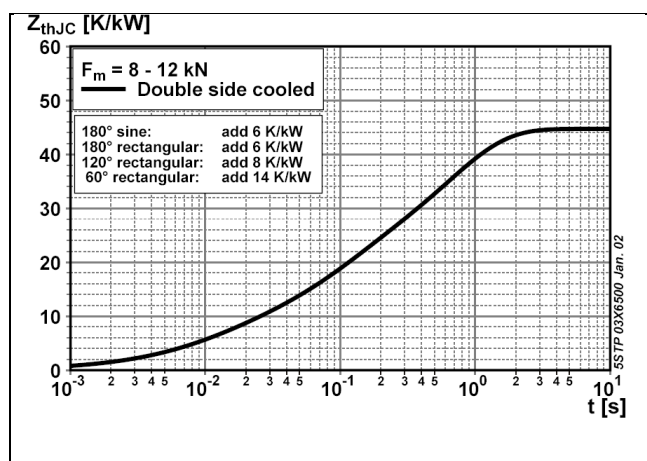


Fig. 1 Transient thermal impedance junction-to case.

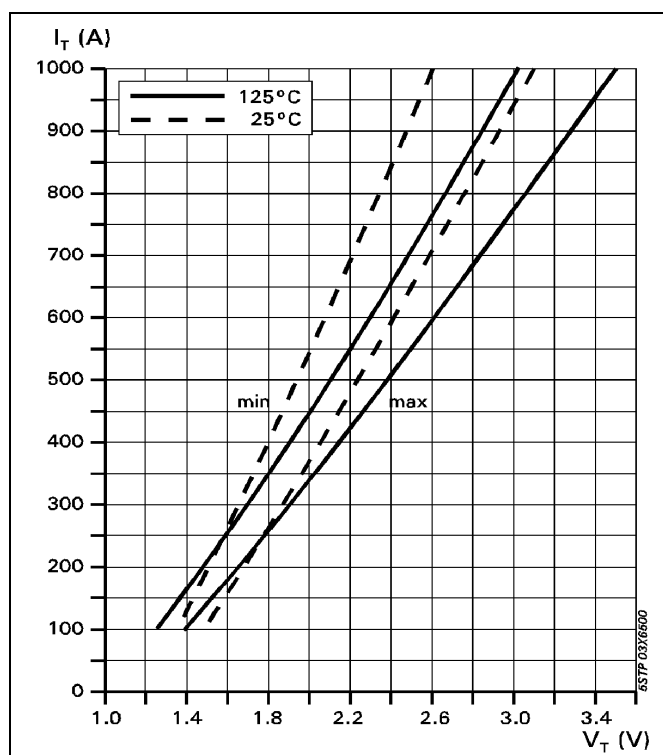


Fig. 2 Max. on-state voltage characteristics

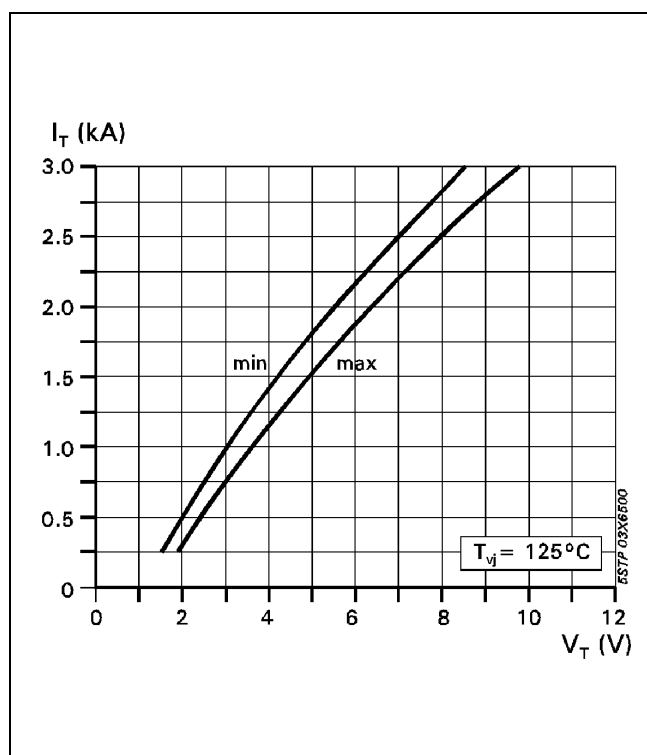
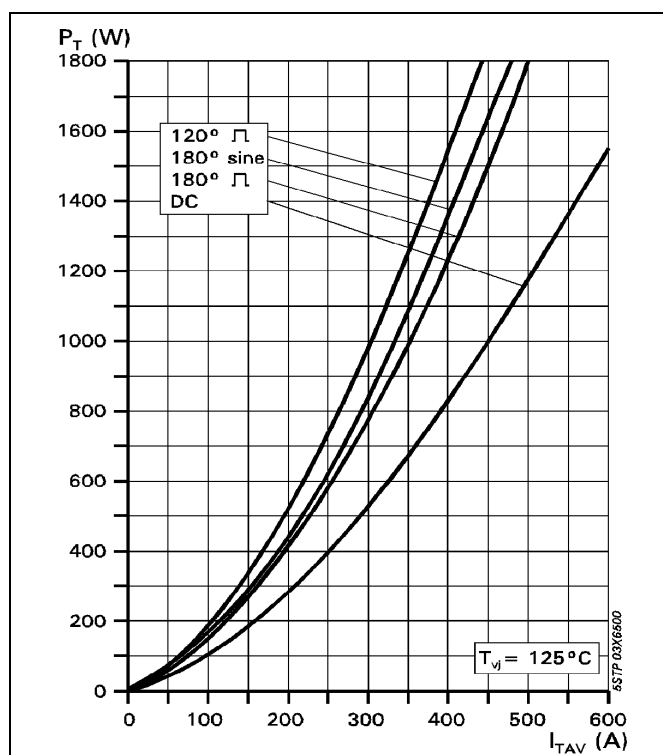
Fig. 3 On-state characteristics.
 $T_{vj}=125^{\circ}\text{C}$, 10ms half sine

Fig. 4 On-state power dissipation vs. mean on-state current. Turn-on losses excluded.

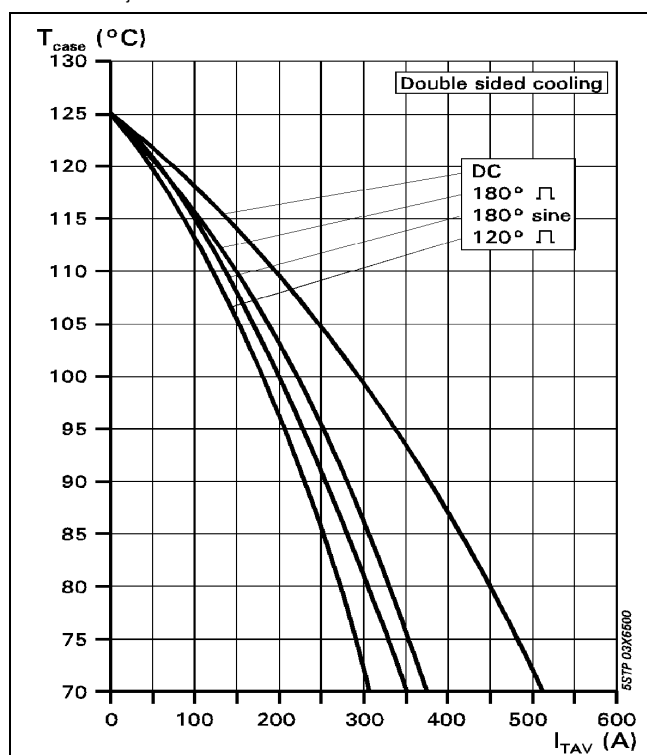


Fig. 5 Max. permissible case temperature vs. mean on-state current.

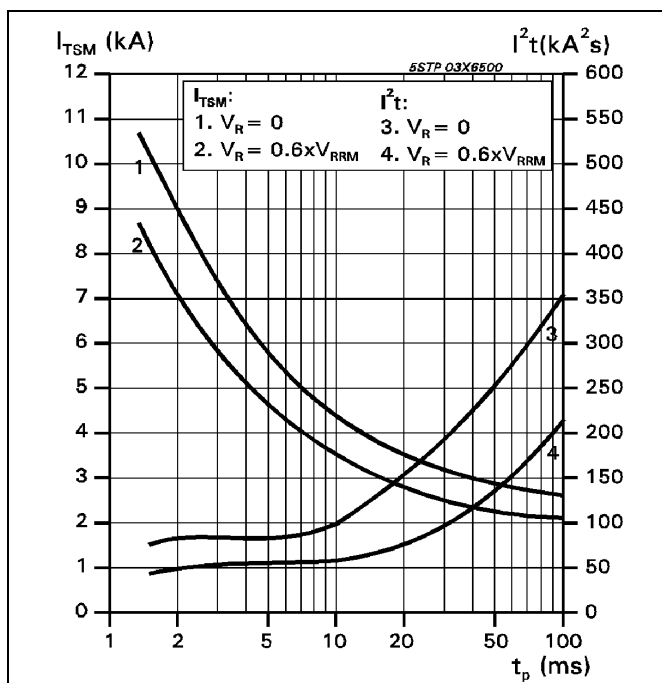


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

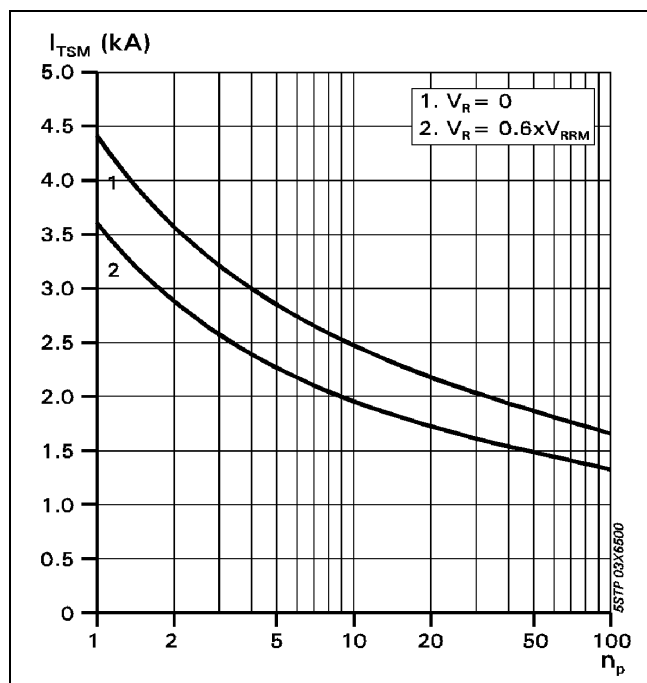


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

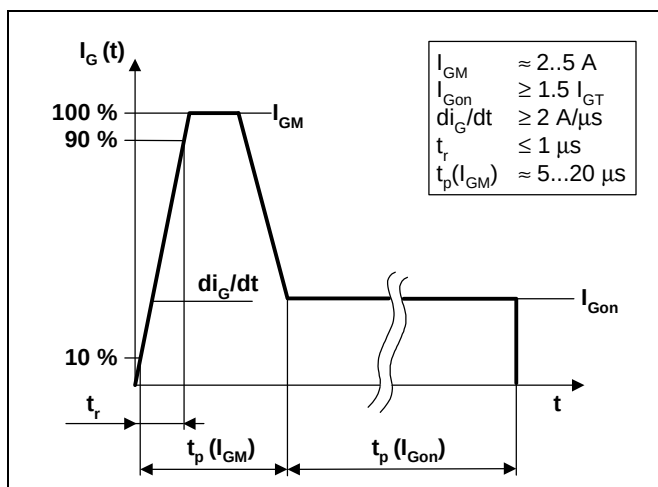


Fig. 8 Recommended gate current waveform.

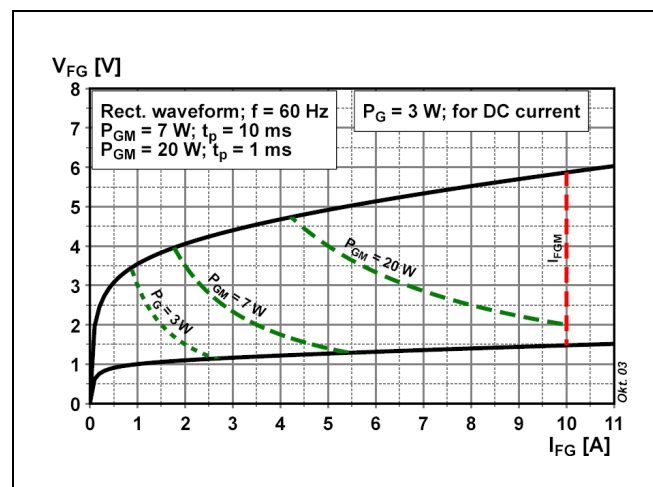


Fig. 9 Max. peak gate power loss.

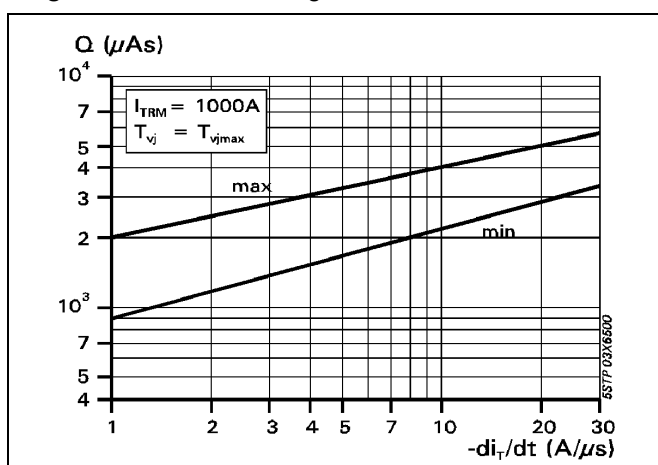


Fig. 10 Recovery charge vs. decay rate of on-state current.

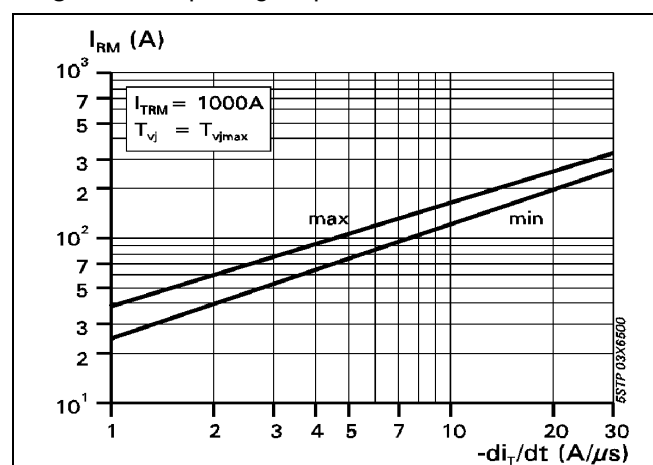


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

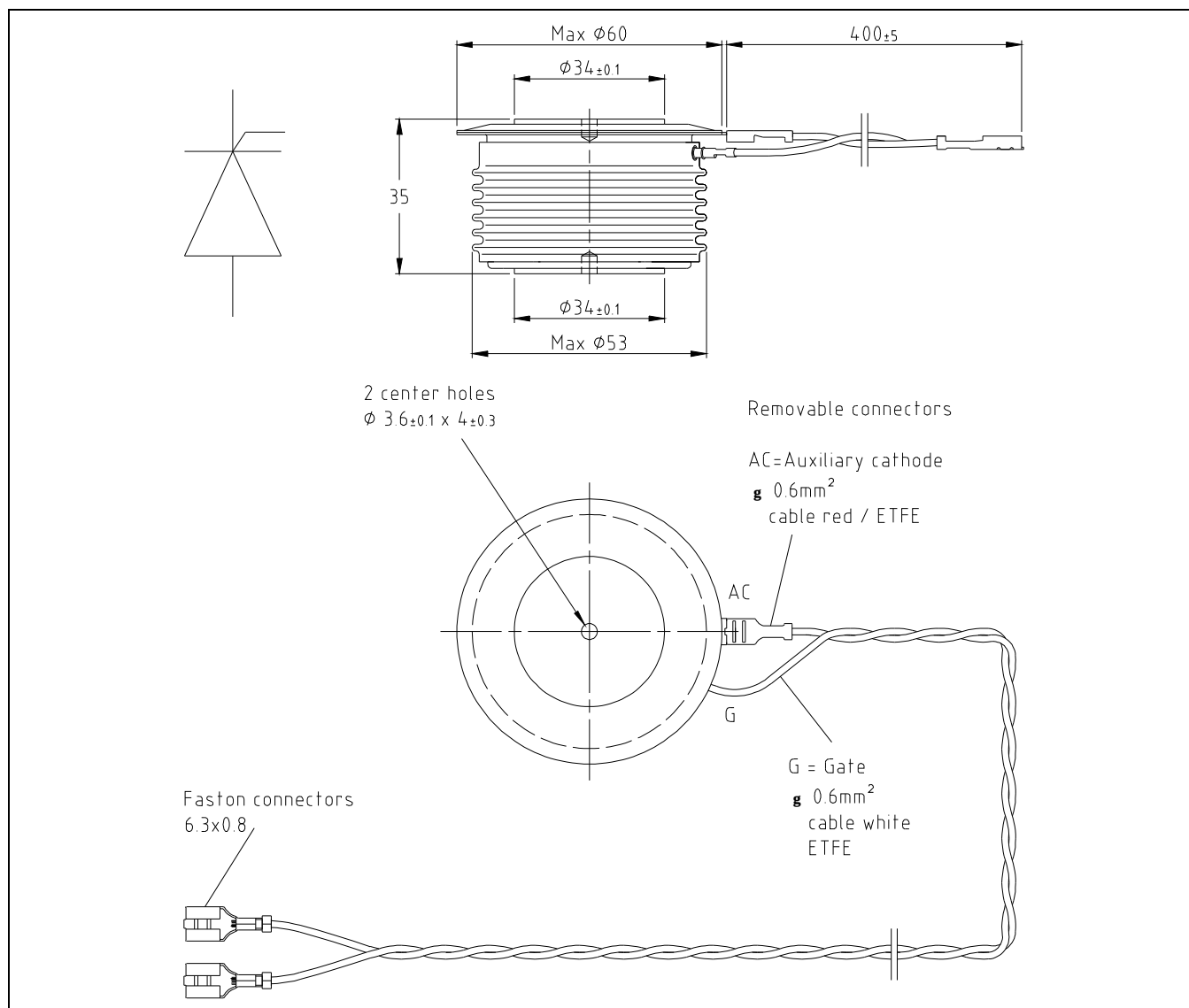


Fig. 12 Device Outline Drawing.

Related application notes:

Doc. Nr	Titel
5SYA2020	Design of RC-Snubber for Phase Control Applications
5SYA2034	Gate-drive Recommendations for PCT's
5SYA 2036	Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors
Please refer to http://www.abb.com/semiconductors for actual versions.	

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